CLAIM LISTING

Claim 1 (Previously presented) An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising an amorphous hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, and tantalum oxide.

Claim 2 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a perovskite.

Claim 3 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a material with a dielectric constant of 20 or more.

Claim 4 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a ferroelectric material.

Claim 5 (Original) An integrated circuit as in claim 1 wherein said metal oxide comprises a layered superlattice material.

Claim 6 (Original) An integrated circuit as in claim 5 wherein said layered superlattice material comprises one or more of the following chemical elements: strontium, calcium, barium, bismuth, lead, yttrium, scandium, lanthanum, antimony, chromium, thallium, titanium, tantalum, hafnium, tungsten, niobium, zirconium, oxygen, fluorine and chlorine.

Claim 7 (Original) An integrated circuit as in claim 6 wherein said layered superlattice material comprises a material selected from the group comprising strontium bismuth tantalate, strontium bismuth niobate and solid solutions thereof.

Claim 8 (Original) An integrated circuit as in claim 7 wherein said layered superlattice material comprises strontium, bismuth, tantalum and niobium in relative molar proportions corresponding to the stoichiometric formula $SrBi_y(Ta_{1-x}Nb_x)_2O_9$, wherein $0 \leq x \leq 1$ and $2.0 \leq y \leq 2.2$.

Claim 9 (Canceled)

Claim 10 (Previously presented) An integrated circuit as in claim 1 wherein

said hydrogen barrier layer comprises amorphous strontium tantalate.

Claim 11 (Original) An integrated circuit as in claim 1 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

Claim 12 (Original) An integrated circuit as in claim 11 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

Claim 13 (Original) An integrated circuit as in claim 12 wherein said ferroelectric material comprises a layered superlattice material.

Claim 14 (Original) An integrated circuit as in claim 1 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

Claim 15 (Original) An integrated circuit as in claim 14 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

Claim 16 (Original) An integrated circuit as in claim 15 wherein said ferroelectric material comprises a layered superlattice material.

Claim 17 (Previously presented) An integrated circuit as in claim 1 wherein said amorphous hydrogen barrier layer material is between 30 nanometers and 100 nanometers (nm) thick.

Claim 18 (Previously presented) An integrated circuit as in claim 17 wherein said amorphous hydrogen barrier layer material is between 70 nm and 90 nm thick.

Claim 19 (Canceled)

Claim 20 (Original) An integrated circuit as in claim 1 wherein said integrated circuit includes a semiconducting substrate, and said metal oxide material is located between said hydrogen barrier layer and said substrate.

Claim 21 (Original) An integrated circuit as in claim 20 wherein said integrated circuit includes a wiring layer and a second hydrogen barrier layer located above said wiring layer.

Claim 22 (Original) An integrated circuit as in claim 1 wherein said integrated

circuit further includes a substrate and a wiring layer, said metal oxide material is located between said wiring layer and said substrate, and said hydrogen barrier layer is located above said wiring layer.

Claim 23 (Previously presented) An integrated circuit as in claim 1 further comprising a supplemental hydrogen barrier layer, said supplemental hydrogen barrier layer containing supplemental hydrogen barrier layer material different from said amorphous hydrogen barrier layer material.

Claim 24 (Previously presented) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer material comprises silicon nitride or aluminum oxide.

Claim 25 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is conducting.

Claim 26 (Original) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is insulating.

Claim 27 (Previously presented) An integrated circuit as in claim 23 wherein said supplemental hydrogen barrier layer is adjacent to and in direct contact with said hydrogen barrier layer containing said amorphous hydrogen barrier layer material.

Claim 28 (Previously presented) An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising an amorphous hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide, wherein at least a portion of said amorphous hydrogen barrier layer material directly contacts said thin film of metal oxide material.

Claim 29 (Original) An integrated circuit as in claim 28 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

Claim 30 (Original) An integrated circuit as in claim 29 wherein said

capacitor is a ferroelectric capacitor and said metal oxid comprises a ferroel ctric material.

Claim 31 (Original) An integrated circuit as in claim 30 wherein said ferroelectric material comprises a layered superlattice material.

Claim 32 (Original) An integrated circuit as in claim 28 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

Claim 33 (Original) An integrated circuit as in claim 32 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

Claim 34 (Original) An integrated circuit as in claim 33 wherein said ferroelectric material comprises a layered superlattice material.

Claim 35 (Previously presented) An integrated circuit as in claim 28 wherein said amorphous hydrogen barrier layer material is between 30 nanometers and 100 nanometers (nm) thick.

Claim 36 (Original) An integrated circuit as in claim 28 wherein said amorphous material has a crystallization temperature of greater than 650°C.

Claim 37 (Previously presented) An integrated circuit as in claim 28 wherein said integrated circuit further comprises a supplemental hydrogen barrier layer that includes crystalline material.

Claims 38 – 68 (Canceled)

Claim 69 (Previously presented) An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising an amorphous hydrogen barrier layer material selected from the group consisting of: strontium tantalate, bismuth tantalate, tantalum oxide, titanium oxide, zirconium oxide and aluminum oxide;

wherein no silicon-containing material is located between said amorphous hydrogen barrier layer material and said thin film of metal oxide material.

Claim 70 (Previously presented) An integrated circuit as in claim 69 wherein said integrated circuit comprises a capacitor having a first electrode and a second electrode, and said metal oxide material is located between said first and second electrodes.

Claim 71 (Previously presented) An integrated circuit as in claim 70 wherein said capacitor is a ferroelectric capacitor and said metal oxide comprises a ferroelectric material.

Claim 72 (Previously presented) An integrated circuit as in claim 71 wherein said ferroelectric material comprises a layered superlattice material.

Claim 73 (Previously presented) An integrated circuit as in claim 69 wherein said integrated circuit comprises a field effect transistor (FET) comprising a substrate and a gate electrode, and said metal oxide material is located between said substrate and said gate electrode.

Claim 74 (Previously presented) An integrated circuit as in claim 73 wherein said FET is a ferroelectric FET and said metal oxide material comprises a ferroelectric material.

Claim 75 (Previously presented) An integrated circuit as in claim 74 wherein said ferroelectric material comprises a layered superlattice material.

Claim 76 (Previously presented) An integrated circuit as in claim 69 wherein said amorphous hydrogen barrier layer material is between 30 nanometers and 100 nanometers (nm) thick.

Claim 77 (Previously presented) An integrated circuit as in claim 69 wherein said amorphous material has a crystallization temperature of greater than 650°C.

Claim 78 (Previously presented) An integrated circuit as in claim 69 wherein said amorphous hydrogen barrier layer material is included in a primary hydrogen barrier layer; and

wherein said integrated circuit further comprises a supplemental hydrogen barrier layer that includes crystalline material.

Claim 79 (Previously presented) An integrated circuit as in claim 78 wherein

said supplemental hydrogen barrier layer is located in contact with said primary hydrogen barrier layer.

Claim 80 (Previously presented) An integrated circuit as in claim 78 wherein said supplemental hydrogen barrier layer is insulating.

Claim 81 (Previously presented) An integrated circuit as in claim 78 wherein said amorphous hydrogen barrier layer material is more compatible than said supplemental hydrogen barrier layer with said metal oxide material, and said amorphous hydrogen barrier layer material is located closer than said supplemental hydrogen barrier layer to said metal oxide material.

Claim 82 (Previously presented) An integrated circuit as in claim 78 wherein said amorphous material comprises one of the metal elements that is in said metal oxide material.

Claim 83 (Previously presented) An integrated circuit as in claim 82 wherein said metal oxide material is a layered superlattice material.

Claim 84 (Previously presented) An integrated circuit as in claim 78 wherein said supplemental hydrogen barrier layer comprises a material selected from the group consisting of silicon nitride and aluminum oxide.

Claim 85 (Previously presented) An integrated circuit comprising:

a thin film of metal oxide material; and

a hydrogen barrier layer located to inhibit the diffusion of hydrogen to said metal oxide material, said hydrogen barrier layer comprising strontium tantalate formed from a liquid metal organic precursor in a process using MOCVD conducted at a temperature in a range of from 300°C to 650°C.

Claim 86 (Previously presented) An integrated circuit as in claim 85 wherein said strontium tantalate is formed in a process using MOCVD conducted at a temperature in a range of from 400°C to 500°C.